Overcoming the Challenges of Silicon Carbide to **Ensure Application Success**

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Pushing innovation to create intelligent power and sensing technologies that solve the most challenging customer problems.

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Introduction

Silicon has traditionally been the cornerstone of semiconductor technology. However, silicon has its limitations especially in power electronics, where designers increasingly face new challenges. One way to address silicon's limitations is with wide bandgap semiconductors.

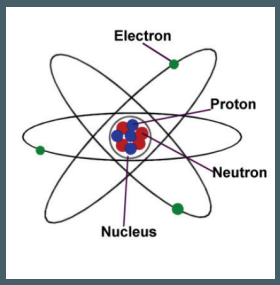
Wide Bandgap Semiconductors

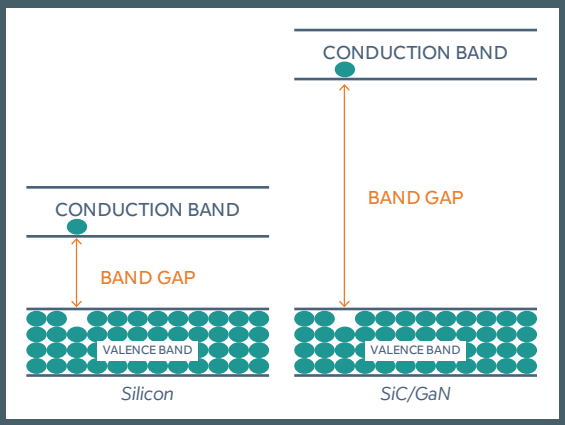
As the name implies, wide bandgap semiconductors such as **silicon carbide (SiC)** and **Gallium Nitride (GaN)** describe a class of semiconductors by their most important electrical property, their bandgap. Bandgap is the difference in energy between the top of the valence band and the bottom of the conduction band. Semiconductors like silicon have a relatively narrow bandgap in the range of 0.6-1.5 electronvolts (eV). (Figure 1)

Bandgap = Energy required to move an electron from its' outer shell, so it can move freely inside the material

Material	Symbol	Bandgap Energy (eV)
Geranium	Ge	0.7
Silicon	Si	1.1
Gallium Arsenide	GaAs	1.4
Silicon Carbide	SiC	3.3
Zinc Oxide	ZnO	3.4
Gallium Nitride	GaN	3.4
Diamond	C	5.5

Wide Band gap





Energy required to move electron from Valence band to Conduction band

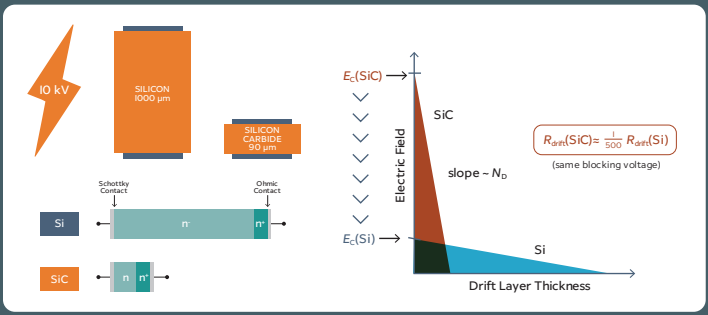
More energy required to move electron

Figure 1: Wide Bandgap Physical Properties

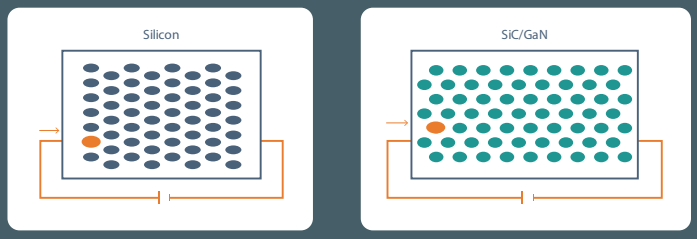
Wide bandgap materials possess bandgaps above 2 eV. Opportunities for wide bandgap semiconductors, which behave more like insulators, are growing because the larger bandgap semiconductors have characteristics that are superior to silicon for many power applications. For example, wide bandgap semiconductors can function at higher voltages, higher frequencies, and higher temperatures. (Figure 2) This makes them ideal in high voltage and high power applications such as *a traction inverter in electric vehicles (EVs)* where fast switching functions and high voltage operation are required to convert a direct current (DC) supply from a vehicle's batteries into an alternative current (AC). Because of material properties, SiC based inverter would extend EV range.

Wide Bandgap Technology

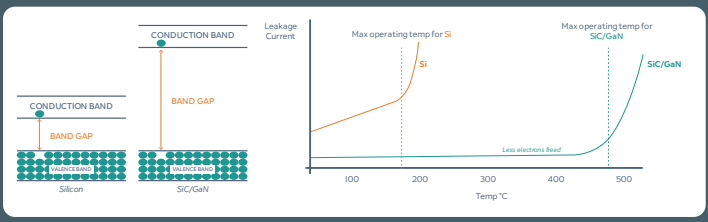
10x Higher Dielectric Breakdown Field Strength
- SiC thickness can be reduced
- Reduces electrical & thermal resistance = Lower Power Losses



2x Higher Electron Saturation Velocity
- Higher switching speeds can be achieved
- Electron Saturation Velocity = max speed of electron



Reduced Leakage Currents
- Provides a stable/low leakage over large temperature range
- Higher energy required to 'free' electrons



3x Higher Thermal Conductivity
- High dissipation of heat from SiC results in lower operating temperature and thermal stress
- SiC allows faster transfer of excited electrons (heat)

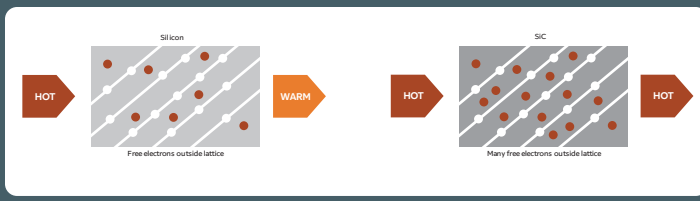
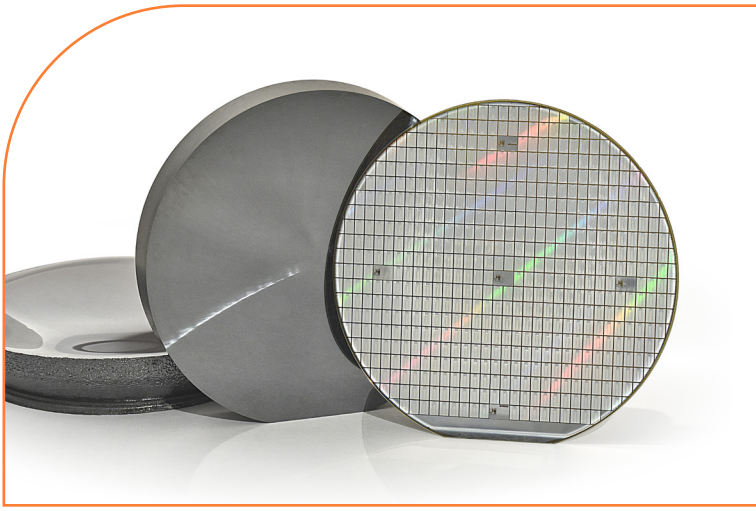


Figure 2: Advantages of Wide Bandgap

Silicon Carbide



Among the wide bandgap semiconductors, silicon carbide (SiC) has emerged as the material with some of the most attractive characteristics for high power conversion applications including *traction inverter* and *on-board charger in EVs*, energy infrastructure applications such as *DC fast charging, solar inverters, energy storage,* and *UPS*.

SiC has been bulk manufactured for more than a century, primarily thanks to its utility as an abrasive. Fortunately, it also turns out to have excellent characteristics for high voltage and high power applications. For example, its physical properties include high thermal conductivity, high saturation electron drift velocity, and a high breakdown electric field. (Figure 3) As a result, systems built with SiC are characterized by extremely low losses and faster switching speeds. Moreover, they can deliver these benefits with smaller geometries than, silicon MOSFET and IGBT devices.

Properties	Si	4H-SiC	GaN
Bandgap Energy (eV)	1.12	3.26	3.50
Electron Mobility (cm2/Vs)	1400	900	1250
Hole Mobility (cm2/Vs)	600	100	200
Breakdown Field (MV/cm)	0.3	2.0	3.5
Thermal Conductivity (W/cm°C)	1.5	4.9	1.3
Maximum Junction Temperature (°C)	150	600	400

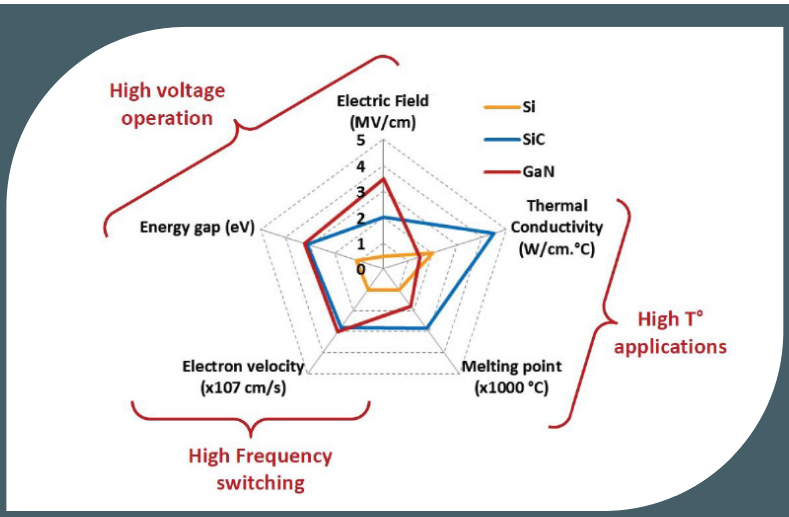


Figure 3: Silicon vs. Wide Bandgap Material Properties

Capable of operating effectively beyond the limits of silicon, SiC also provides a substantial increase in power density when operated at higher frequency than silicon IGBTs. (Figure 4)

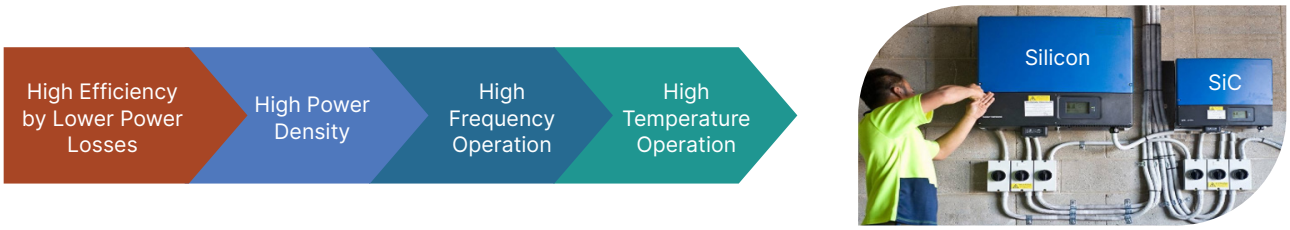


Figure 4: SiC vs. Silicon

SiC and the Opportunities it Enables

For many manufacturers, SiC is being considered as a source of competitive advantage and an opportunity to build energy efficient systems as well as reduce overall system size, weight and costs. This is because SiC based systems are typically more energy efficient, smaller, and generally more robust than silicon based alternatives, thus designers can reduce passive component size and cost. More specifically, SiC devices can run cooler for a given application than alternatives because of its lower heat generation. (Figure 5)

Part of the consideration is implementing new die attach technologies (e.g., *sintering*) which play a role in helping to remove heat from devices and ensure reliable interconnection. SiC devices can operate at much higher voltage and provide faster switching compared to silicon. All of these factors allow designers to take a clean slate approach, rethinking how to achieve optimal functionality at a system level price point that is more appealing to the market.

Some of the high-performance roles in which SiC has already been leveraged include SiC diodes, SiC MOSFETs as well as SiC modules.

Material Properties		
Properties	Si	4H-SiC
Breakdown Field (MV/cm)	0.3	3
Band Energy (eV)	1.12	3.26
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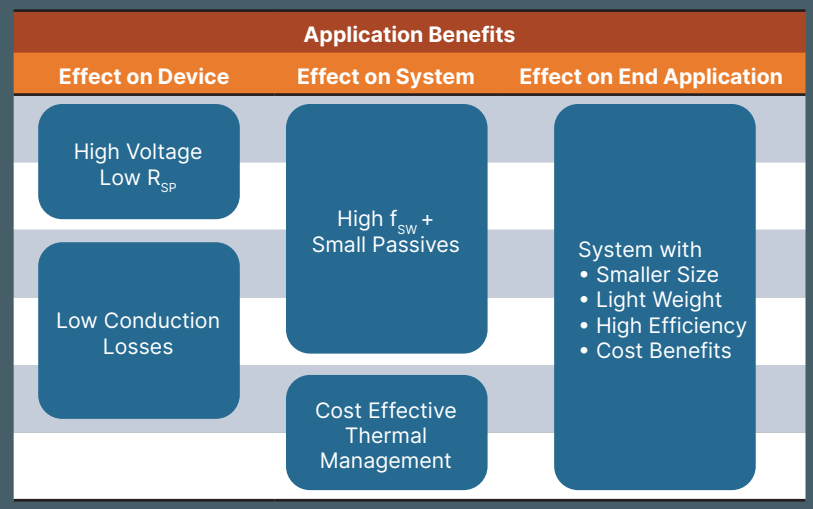


Figure 5: SiC Application Benefits

The superior performance of SiC compared to silicon opens the door to new and emerging applications. SiC devices are designed for 650V and higher. It is at 1200V and higher that SiC becomes the best solution for a wide variety of applications. Applications like solar inverters, EV chargers and industrial AC to DC conversion will all migrate to SiC over the long term. Another long-term application is the *solid-state transformer,* where the current copper and magnet transformer is replaced with semiconductors.

Challenges to Manufacturing SiC

While SiC presents tremendous market opportunities, it comes with its manufacturing challenges. The challenges start with ensuring the purity of the raw material, technically called granulate or SiC powder, generating consistent SiC boules (Figure 6), and then acquiring practical experience in every subsequent processing step needed to deliver a reliable end-product. (Figure 7)

One of unique challenges of SiC is that the material doesn't exist in a liquid phase, so crystals can't be grown from a melt. Crystal growth must be managed with carefully controlled pressure, which makes it more challenging to manufacture than silicon. If SiC is held at a high temperature and low pressure, it dissociates into gaseous species without passing through the liquid phase. Due to this behavior, SiC crystals are grown using a vapour phase technique called sublimation, or physical vapour transport (PVT). SiC powder is placed in a crucible inside the furnace and heated to a high temperature (above 2200°C), then the SiC sublimes and crystallizes on a seed to form a SiC crystal. For growing material using this method, an essential ingredient is a seed crystal with a diameter similar to that of the boule. With PVT, growth rates are very slow in the range of 0.1-0.5 mm/hour.

Figure 6: SiC Powder, Boule, and Wafer

Likewise, even the process of creating wafers is made more challenging by the extreme hardness of SiC compared to silicon. SiC is a very hard material and difficult to cut, even with a diamond saw. Its diamond-like hardness is different from many other semiconductors. Several other methods exist for separating an ingot into wafers, but these methods can introduce defects into the single crystal.

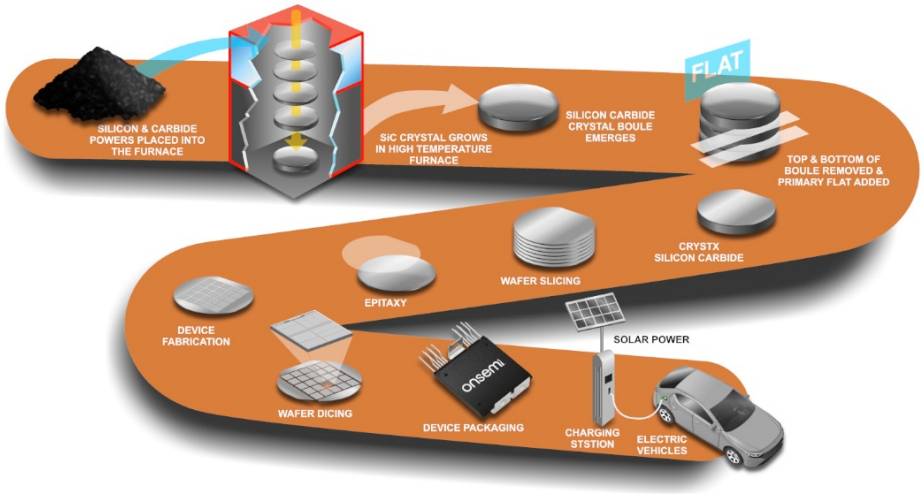


Figure 7: SiC manufacturing from raw material to end-product

There is also scaling challenges. Compared with silicon, SiC is a highly defective material. SiC doping is a difficult process, and the challenge of producing larger SiC wafers with fewer defects has kept manufacturing and processing costs high. It is therefore essential to offer a good development process from the start to maintain a uniform quality output. Nevertheless, 8-inch substrates are beginning to penetrate the market and **onsemi** is supporting this trend.

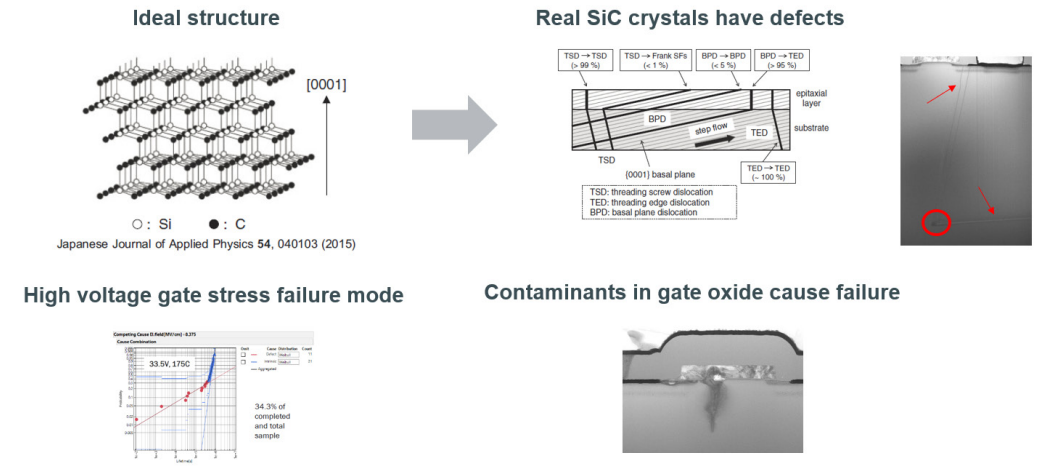


Figure 8: Challenges – SiC Wafers and Defects

Fortunately, companies have invested heavily in mastering this process and achieving consistent and reliable boules and wafers. They have also leveraged their existing experience manufacturing silicon to help in terms of methodology and the underlying material science. Multiple crucial elements must be combined when safely releasing a product to the market. To respond this, SiC standards development is underway. Multiple sub-teams within the Joint Electron Device Engineering Council (JEDEC), the Automotive Electronics Council (AEC), and the European Center for Power Electronics Automotive Qualifying Group (AQG) are doing the fundamental work needed to create SiC standards for the industry. **onsemi** is an active participant in these standards development. This includes the AEC groups and the JEDEC committee JC-70.2 SiC Power Electronic Conversion Semiconductor Standards.

Figure 9: Definition of Robust Intrinsic and Extrinsic Reliability

An Ecosystem Evolves Around SiC

Progress isn't confined to just industry players. There are numerous universities and research centers examining various SiC-specific challenges which include the following:

- Ruggedness with regard to cosmic rays
- Intrinsic lifetime modeling with regard to gate oxide
- SiC/SiO2 interface characterization and lifetime modeling
- Extrinsic population (screening)
- Epitaxy and substrate defectivity
- Body diode degradation
- High-voltage blocking reliability (HTRB)
- Specific performance metrics with regard to edge termination, avalanche robustness, and short circuit
- Design for high dv/dt ruggedness
- Surge current.

In further support of this ecosystem, the Pennsylvania State University (PSU) and **onsemi** signed a memorandum of understanding (MoU) toward an $8 million strategic collaboration that includes the establishment of the **onsemi** Silicon Carbide Crystal Center (SiC3) at PSU's Materials Research Institute. **onsemi** committed to funding SiC3 with $800,000 per year. We also work with many other SiC researchers including University Gent, TU Wien, University of Antwerp, University of Bremen, University of Iceland, and University of Padua. (Figure 10)

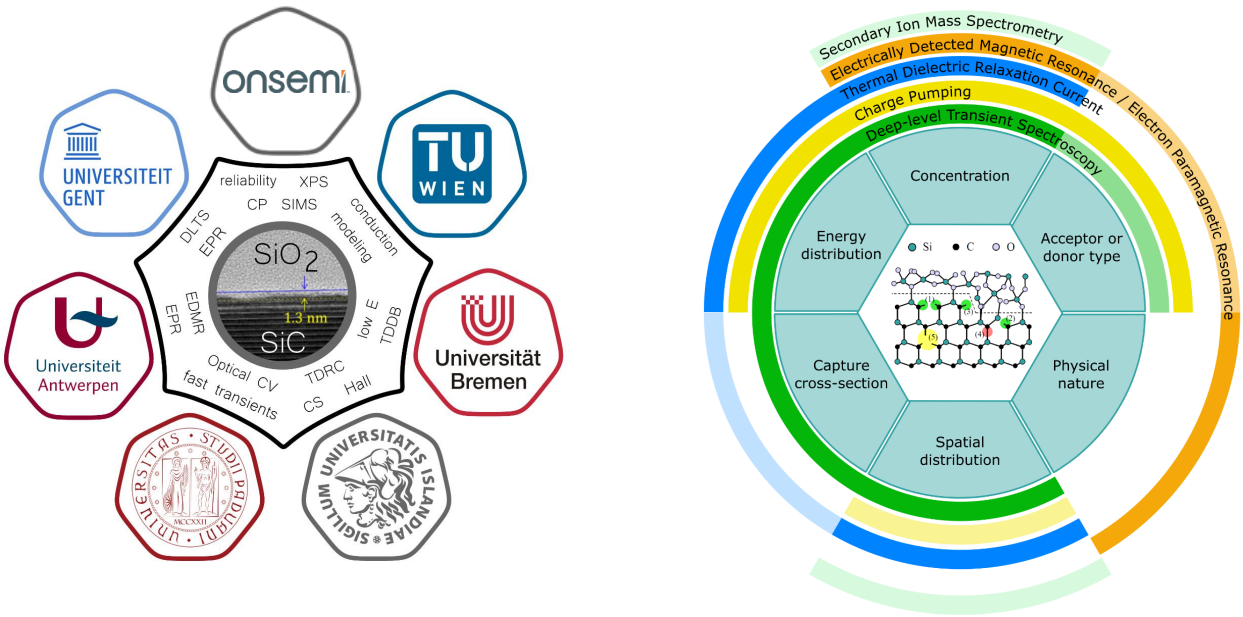


Figure 10: Collaboration with Universities and Research Centers – SiC/SiO2 Interface

The onsemi Advantage in SiC Semiconductor Production

As a vertically integrated supplier with deep application expertise, **onsemi** leverages years of experience in every aspect of semiconductor production. This includes a quality methodology working toward zero defects (Figure 11), robust performance, and a unique perspective on what it takes to deliver results from boule to customer.

Figure 11: **onsemi** Quality – Road to Zero Defects

"Vertical integration in SiC wafer and device manufacturing can improve yield by five to ten percentage points."
– McKinsey Article

The **onsemi** supply chain begins by growing its own single crystal SiC material at its Hudson, New Hampshire facility. A thin epi layer is then produced on the in-house substrate.

This material continues through several device processing steps to the packaging of final products. This end-to-end approach facilitates the fullest possible testing and root cause analyses, yielding very high reliability and zero-defect products.

Having a vertically integrated supply chain offers many advantages. For example, according to a recent McKinsey article, "vertical integration in SiC wafer and device manufacturing can improve yield by five to ten percentage points."

It is also simpler to scale production when there is visibility into and control over every step. Cost control, likewise, is a benefit since the whole process can be optimized at every step, with accountability and a clear sense of how each step impacts the others.

The onsemi Process

This 5-steps methodology is applied at **onsemi** to address SiC specific challenges, including (but not limited to):

- Substrate and epitaxy defectivity level. Gate oxide: intrinsic lifetime modeling (SiC/SiO2 interface characterization) and extrinsic population (screening) (see page 11-12 for more information)
- Body diode degradation
- Reliability during high-voltage blocking (HTRB)
- Application-related performance (avalanche robustness, edge termination, short circuit, ruggedness against cosmic rays, design for high dv/dt ruggedness, and surge current.)

By making great use of production tools to eliminate any product that would not meet the requirements, this structured approach provides a superior assurance on quality, reliability, and availability. Tools include the following:

- Defect scanning performed before and after epitaxial growth
- In-process defect screenings with coordinate tracking and auto classification
- Wafer level burn-in
- Dynamic pattern average testing
- 100% rated voltage and 175°C test
- 100% avalanche rated.

This proven quality program, combined with vertical integration, creates an opportunity for rapid feedback, quick iteration, and production agility.

The 5-steps applied to Gate Oxide Integrity

When applied to crucial gate oxide integrity (GOI), the detailed quality control elements include:

1 CONTROL

Control methodology and tools are put in place for manufacturing SiC technologies (e.g., control plan, statistical process control, process failure modes and effects analysis (FMEA)). Data is collected and used as a foundation for potential process improvements.

2 IMPROVE

Implement improvements – since substrate or epitaxial defects, metallic contaminants, and particles can heavily impact gate oxide quality, continuous improvements and controlled introduction to production can greatly reduce further occurrence of defects.

3 TEST & SCREEN

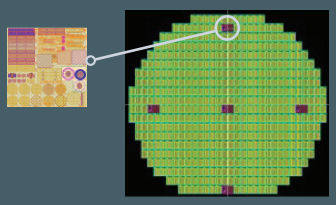
A full suite of visual and electrical screening tools has been developed by **onsemi** to eliminate defective dies.

- Substrate scans and additional scans performed during the wafer fab processing identify all defects with coordinates and auto-classification. These multiple inspections allow excluding defects found through other steps, and help identify any additional potential process marginality at critical process steps. All flagged defects found in the inspections above are excluded from the population.
- Electrical screening is implemented at multiple levels (Figures 12 & 13):
  - Wafer level performance and acceptance (parametric testing and gate oxide integrity acceptance criteria)
  - Wafer level burn-in
  - Wafer level die sort
  - Dynamic part average testing is in place to remove electrical outliers.

Finally, all wafers are screened with 100% automated outgoing inspection.

Electrical Test Sequence

Wafer acceptance test
- QBD (Gate oxide integrity)
- Process module verifications (Rsheet, junction Ivs, Alignments, Uniformities)
- Mini FETs and Diodes



Sequence wafer-level test
- Pre I_{GSS}, I_{DSS}
- Unclamped Inductive Switching test
- Gate stress pulse
- I_{GSS}
- V_{th} (several extraction currents)
- I_{DSS}
- BV_{DSS} (several extraction currents)
- R_{ON} (several extraction currents)
- V_{SD} (several extraction currents)
- R_g

Sequence package test
- Pre I_{GSS}, I_{DSS}
- Switching test at nominal current
- Unclamped Inductive Switching test
- Gate stress pulse
- I_{GSS}
- V_{th} (several extraction currents)
- I_{DSS}
- BV_{DSS} - R_{ON} - V_{SD} (several extraction currents)
- R_g

Figure 12: Electrical Test Sequence

Burn-in process required to address early failures

Package Level Burn-in (PLBI) system:

- Burn-in conditions technology specific
- T_{stress}>100C
- V_{GS}>V_{GS_max}
- Time to Failure tracing (in situ monitoring)

Wafer Level Burn-in (WLBI) system

- Similar burn-in conditions than PLBI
- Time to Failure tracing (in situ monitoring)
- Multi chamber system
- Single touch down probe cards

Figure 13: Burn-in process required to address early failures

4 CHARACTERIZE

onsemi is using the charge to failure (QBD) as a simple method to compare gate oxide quality independent of the gate oxide thickness. This technique is more refined than GOI/Vramp and will detect finer details in the intrinsic distribution.

SiC and Si gate oxides have comparable intrinsic capabilities in breakdown and lifetime. A side-by-side comparison of intrinsic QBD performance (independent of gate oxide thickness) shows **onsemi** planar SiC being 50 times better intrinsically than Si for the same nominal thickness.

In production, the gate oxide quality of each lot is evaluated by sampling charge to failure (QBD) for SiC MOSFET product dies and compared with large area (2.7 mm x 2.7 mm) NMOS capacitors.

An acceptance criterion is in place to accept or reject at the wafer level.

5 QUALIFY & EXTRACT MODELS

Determining the true current conduction mechanism(s) of the gate oxide is crucial when defining the stressing conditions. Thermally assisted tunneling competes with Fowler Nordheim as a function of stressing electric fields and stressing temperature. Therefore, understanding the conduction mechanisms prevents stress in another conduction mode than the one representative of actual use conditions in the field.

The intrinsic performance of the gate oxide is assessed via time-dependent dielectric breakdown (TDDB) stressing. Gate bias and temperature are combined to stress the SiC MOSFETs, and times-to-failures are recorded. Weibull statistical distributions are then used to extract the lifetimes.

A very conventional approach has been used so far: Arrhenius temperature acceleration and E model for the gate voltage. Additional studies are ongoing to refine the model; the E model is considered too conservative. Stresses at lower oxide fields and long duration (with 63% of several months to more than a year) are being conducted, and they should experimentally confirm which model best suits the data.

SiC Application Success with onsemi, the onsemi difference

onsemi uniquely recognizes the critical role of SiC in the future of power electronics. Consequently, the company is investing in capacity and innovations to ensure SiC achieves its full potential as quickly as possible. We own end-to-end SiC manufacturing process from raw material to end product, in which there are a lot of steps that many companies in the industry are unable to do, however one of our strengths is our capability to control the process from start to finish to ensure quality of SiC product to our customers.

Leveraging its leading position, technologies and expertise in MOSFETs and IGBTs, along with high decades of investment in packaging technologies, we understand our customer's unique system requirements and have been offering high performance, application specific EliteSiC product portfolio which was developed under realistic conditions compared with the competition. With our deep application expertise in EVs and industrial, along with our system level PLECS simulation tools, which were developed leveraging novel physically based, scalable SPICE model methodologies, you can rely on us to deliver innovative solutions that provide you a competitive edge and shorten time to market.

More Information:

- **onsemi** Selects the Czech Republic to Establish End-to-End SiC Production for Advanced Power Semiconductors
- **onsemi** Completes Expansion of SiC Production Facility in Bucheon, South Korea
- Walk Through | Complete End-to-End Silicon Carbide Supply Chain
- Silicon Carbide Technology Page
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- Elite Power Simulator
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